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TITLE: Data-pattern induced skew reducer

Brief Summary Text - BSTX (5):

Modem computer systems may contain several microprocessors, microcontrollers, and other digital devices connected to each other by a bus. The bus transports data among the microprocessors and other components. The bus is composed of a number of traces. Traces are wire-like connections that are printed on the circuit board and function as transmission lines.

Brief Summary Text - BSTX (6):

FIG. 1 illustrates a conventional latched driver configuration with a latch 105 and a driver circuit 100 coupled to a transmission line 110. Data that appears at an input terminal 106 to the latch 105 can be placed at an output terminal 107 of the latch 105 after the clock signal has transitioned (i.e., changed states); a positive or negative edge of the clock signal can be used consistently for this purpose. When the data appears at the output terminal 107 of the latch 105 and the driver circuit 100 is enabled, the data is ready to be propagated, allowing a data signal to be transferred to the transmission line 110. If there is a large impedance mismatch between the transmission line 110 and the driver circuit 100, intersymbol interference can occur. The presence of intersymbol interference on a transmission line can cause an increase in the skew and a corresponding decrease in the overall bus transfer rate. Thus, it would be beneficial to have a device that can enhance bus transfer rate by minimizing intersymbol interference.

Brief Summary Text - BSTX (8):

In one aspect of the present invention, a skew reducer to minimize the uncertainty of the data window at the receiver caused by intersymbol interference is provided. The skew reducer includes a memory with a data input terminal and an output terminal, and is adapted to receive and record the immediate history of the data stream driven out from the core. A logic circuit has an input terminal coupled to receive at least a portion of the bits in the memory, and an output terminal coupled to deliver a first signal in response to the digital signal having a first predetermined pattern, and deliver a second signal in response to said digital signal having a second predetermined pattern. A first delay path is coupled to receive the digital signal. A multiplexer has a first input terminal coupled to the first delay path, a second input terminal coupled to receive the digital signal, and an enable coupled to the output terminal of the logic circuit.

Detailed Description Text - DETX (4):

As previously mentioned, modem computer systems generally contain numerous components (e.g., a microprocessor, disc drive, monitor, keyboard, CD drive, etc.) that communicate with each other. Thus, there is normally a large number of data transfers occurring during any given time. In most modem computer systems, data is in the form of bits (i.e., binary digits). Bits are typically stored as voltages. When positive logic is used, a bit value of one (i.e., a one) is generally stored as a high voltage, while a bit value of zero (i.e., a zero) is generally stored as a low voltage. A high voltage, as defined in this application, is a voltage equal to the voltage V.sub.CC when used "on chip" and V.sub.ddq when used for the input/output circuits. A low voltage is a voltage level equal to the ground voltage.

Detailed Description Text - DETX (5):

FIG. 2A is an equivalent circuit representation of a transmission line 200, which can be used to send information from one location to the other. Generally, current is sent from one location along a top rail 203 to a second location, and return current is sent back to the first location along a bottom rail 204. Associated with both rails 203, 204 are several inductors 207 and capacitors 208 which constitute an ideal transmission line having

impedance Z.sub.0. As the current continues to progress down the transmission line 200, data is continually stored on corresponding capacitors 208. In this manner, data can be sent from one location to the other.

Detailed Description Text - DETX (7):

Within a computer system, a conventional driver (i.e., a transmitter) 300 and a receiver 305 are generally used to drive and sense data on the transmission line 200, as shown in FIG. 3. The impedance of the transmission line 200 is represented by Z.sub.0, as previously mentioned. The transmission line 200 is connected to the driver 300 along a line 307 and to the receiver 305 along a line 308. Typically, drivers transfer digital signals on a transmission line 200 by connecting the transmission line 200 to a voltage source. Digital signal, as defined in this applications, refers to either a data signal, clock signal, or a strobe signal. The voltage source may generate the voltage V.sub.ddq which may be different from the voltage V.sub.CC, while the voltage V.sub.SS may be a ground voltage. The driver 300 can be modeled simplistically as an impedance Z.sub.up associated with a voltage V.sub.ddq and an impedance Z.sub.down associated with a voltage V.sub.SS. A switch 310 can be used to connect the line 307 to either the voltage source 302 or the voltage source 303. The switch 310 may be controlled by an enable signal (not shown). If the enable is "on", the buffer is active otherwise the driver is in a high impedance state.

Detailed Description Text - DETX (15):

FIG. 4A illustrates a first embodiment of a skew reducer 400 in accordance with the invention. The skew reducer 400 includes three storage elements (e.g., latches, flip-flops, etc.) 405, 410, and 415, which all have an enable input terminal CLK coupled to a clock signal line 403 and a reset input terminal RESET which may be user controlled, and the input terminals of the latches would reflect this state. Thus, the latches 405, 410, and 415 pass the data from their respective input terminals 406, 411, 416, to their respective output terminals 407, 412, 417 when a clock transition occurs. The output terminal 407 of the latch 405 is connected to the input terminal 411 of the latch 410. Similarly, the output terminal 412 of the latch 410 is connected to the input terminal 416 of the latch 415.

Detailed Description Text - DETX (16):

High and low frequency delay paths 420 and 425 are coupled to the output terminal 407 of the latch 405. The high frequency delay path 420 is a delay path used for data signals that have a high-frequency data pattern. Similarly, the low frequency delay path 425 is a delay path used with data signals that have a low-frequency data pattern. Thus, the signal at the output terminal 407 of the latch 405 is applied to the high-frequency delay path 420, the low frequency delay path 425, and the input terminal 411 of the latch 410. The delay paths 420 and 425 are also connected to the input terminals 436 and 437 of a multiplexer 435. The high and low frequency delay paths 420 and 425 may include several logic devices (e.g., inverters), compensated delay lines, or may be just a wire delay, depending on design interests. One skilled in the art will appreciate that the delay paths 420, 425 as shown in FIG. 4A, are functionally equivalent.

Detailed Description Text - DETX (17):

The data signal at the output terminal 407 of the latch 405 is also applied to one input terminal 431 of an exclusive OR (EX-OR) logic gate 430. The input terminal 431 of the EX-OR gate may also be connected to the input terminal 406 of the latch 405 as shown in FIG. 4E. Alternatively, the EX-OR logic gate 430 could be replaced by a combination of logic devices whose function is essentially the same. The output terminal 417 of the latch 415 is applied to a second input terminal 432 of the EX-OR logic gate 430. The output terminal of the EX-OR logic gate 430 is connected to a select input terminal 438 of the multiplexer 435. Finally, an output terminal 439 of the multiplexer 435 is connected to an input terminal 441 of a driver circuit 440, which is connected to a transmission line 445. The select input terminal 438 of the multiplexer 435 allows either the signal from the high frequency delay path 420 or the low frequency delay path 425 to be transferred to the transmission line 445 by the driver circuit 440.

Detailed Description Text - DETX (18):

If a three bit data stream (e.g., 1-0-1) were present at the input terminal 406 to the latch 405, each bit would individually be recorded in the skew reducer. When the clock transitions, the first data bit (i.e., the first one) would

be transferred to the output terminal 407. The first data bit is applied to the high and low frequency delay paths 420, 425, the input terminal 411 of the latch 410, and the input terminal 431 of the EX-OR logic gate 430.

Detailed Description Text - DETX (19):

As an example, the high-frequency delay path 420 may include six inverters (not shown), the delayed first bit value appears at the input terminal 436 of the multiplexer 435 after a time delay t.sub.HF related to the time that it takes to traverse six inverters. For example, the first data bit may go from a high to a low after passing the through the first inverter in the high frequency delay path 420 in a time 1/6 t.sub.HF. Alternatively, a "low" to "high" transition can also be implemented. Similarly, the same data bit would become a high again after traversing a second inverter after some time delay t.sub.HF /3. After traversing all six inverters, the first data bit would be in a high state and would be at the input terminal 436 of the multiplexer 435 after some delay t.sub.HF. A circuit may also be designed such that the low-to-high and high-to-low delays are different. Similarly, the high-frequency and low-frequency delays may be different where, for example, one delay may be zero and the other a select amount.

Detailed Description Text - DETX (22):

A second clock transition places the second data bit (i.e., the zero in this example) which was at the input terminal 406 of the latch 405 at the output terminal 407 of the latch 405. This data bit is also applied to the input terminals of the high and low frequency delay paths 420, 425 and the input terminal 431 of the EX-OR logic gate 430. The time required for progression of the second bit through the high and low frequency delay paths 420, 425 is the same as it was for the first bit. Almost simultaneously, the first data bit which was at the input terminal 411 of the latch 410 is transferred to the output terminal 412. The first data bit is then applied to the input 416 of the latch 415.

Detailed Description Text - DETX (23):

Finally, a third clock transition places the first data bit which was at the input terminal 416 of the latch 415 at the output terminal 417; the second data bit which was at the input 411 is placed at the output 412 of the latch 410. The third data bit which was at the input 406 is placed at the output 407 of the latch 405, the inputs of the high and low frequency delay paths, and the input 431 of the EX-OR logic gate 430. Thus after three clock transitions, the outputs of the latches 415, 410, 405 corresponding to the first, second, and third bits of the original data stream are 1-0-1, respectively illustrating the recording nature of the skew reducer 400.

Detailed Description Text - DETX (24):

The EX-OR logic gate 430 generates an output on the line 438 after comparing the third data bit (i.e., the one at the output terminal 407) to the first data bit (i.e., the one at the output terminal 417). In this example, the first and third bits are the same (i.e., both are high), which generates a low on the output terminal 438 of the EX-OR gate 430. The low at the output corresponds to the select input 438 of the multiplexer 435. The multiplexer would then allow the passage of the delayed high frequency signal from the high frequency delay path 420 through the multiplexer 435 to the driver circuit 440.

Detailed Description Text - DETX (25):

As would be understood by one skilled in the art, identical first and third bits do not always indicate the data pattern is a high frequency data pattern. For example, an extremely low-frequency data pattern (e.g., 1-1-1-1 and 0-0-0-0) have the same first and third bits but are not a high-frequency data pattern. In this case, the multiplexer 435 would still select the data signal from the high-frequency, delay path to be sent to the driver circuit 440. Though the wrong delay would have occurred, the signal would not cause difficulty at the receiver because the bus would not be transitioning is already in a settled state.

Detailed Description Text - DETX (26):

If the first and third bits are different, the EX-OR logic gate 430 causes the multiplexer 435 to pass the delayed signal from the low frequency delay path 425 to the driver circuit 440. The values used for the high frequency and low frequency delays can be generated from simulation of an actual computer system. For example, the

measurements of specific components in a given circuit can be placed in a simulation program, and the high frequency and low frequency delays needed to minimize skew could be generated.

Detailed Description Text - DETX (27):

The placement of delayed signals on the transmission line by the driver results in an increase valid data time. The valid data time is the sum of the setup and hold times. FIG. 4D is a timing diagram illustrating the data signal that was sent by the driver which is now at the receiver. One is skilled in the art will realize that the signals 470, 480 shown in FIG. 4D are an exploded view of a portion of the signals 490, 495 of FIG. 4C. The data signal 472 indicates the expected data signal, while the second data signal 470 is the actual observed signal and the region labeled 474 is the time difference between the two signals 470, 472. The valid data time 482 is considerably larger than the corresponding time for a conventional logic circuit without a skew reducer. In this example, the high frequency delay path should be delayed by a time t.sub.HF indicated by the region 474 in order to restore the signal back to its expected timing.

Detailed Description Text - DETX (28):

In some implementations, the user may choose to disable the skew reducer 400. Override circuitry 500 is provided to temporarily bypass the skew reducer 400, as shown in FIG. 5. Within the override circuitry 500 is a NOR gate 505. One skilled in the art will appreciate that other types of logic gates that are functionally equivalent to the NOR gate 500 could be used. An enable signal is sent to the override circuitry 500 along a line 510. By placing a high signal on the line 510, the output terminal of the NOR gate 505 is forced low, independent of the status of the output terminal of the EX-OR gate 430. A low signal at the output terminal of the NOR gate 505 forces the multiplexer 435 to select the data signal from the low-frequency, delay path 425. If the low frequency delay path 425 only contains a wire, there would be essentially the same amount of delay in traversing the skew reducer 400 as it would exist in a conventional latching bus structure. Thus, data would have essentially bypass the skew reducer 400.

Claims Text - CLTX (13):

a logic circuit having an input terminal coupled to receive at least a portion of the bits in the memory, having an output terminal to deliver a first signal in response to the digital signal having a first predetermined pattern, and deliver a second signal in response to said digital signal having a second predetermined pattern;

Claims Text - CLTX (15):

a multiplexer having a first input terminal coupled to the first delay path, a second input terminal coupled to receive the digital signal, and an enable coupled to the output terminal of the logic circuit.

Claims Text - CLTX (16):

9. The skew reducer of claim 8, wherein the logic circuit is an EX-OR logic gate.

Claims Text - CLTX (18):

11. The skew reducer of claim 8, including a driver circuit having an input terminal coupled to an output terminal of the multiplexer and an output terminal coupled to a transmission line.

Claims Text - CLTX (20):

13. The skew reducer of claim 10, wherein the memory includes a first and second latch each having a data input terminal, a clock input terminal, and a data output terminal, the data input terminal of the first latch being coupled the receive the digital signal, the data output terminal of the first latch being coupled to the data input terminal of the second latch, the clock input terminals coupled to receive a clock signal, and at least one of the data output terminals of the first and second latches being coupled to the logic circuit and the first and second delay paths.

Claims Text - CLTX (21):

14. The skew reducer of claim 13, wherein the memory includes a third latch having a data input terminal, a clock input terminal, and a data output terminal, the data input terminal of the third latch being coupled to the data output terminal of the second latch, the clock input terminal of the third latch being coupled to a clock signal, and the data output terminals of the first and third latches being coupled to the logic circuit.

Claims Text - CLTX (22):

15. The skew reducer of claim 8, including an override circuit having a first input terminal coupled to the output terminal of the logic circuit, an output terminal coupled to the enable of the multiplexer, and a second input terminal coupled to receive a control signal, said override circuit for delivering a signal in response to receiving the control signal, independent of the value of the signal received from the logic circuit.

Claims Text - CLTX (25):

a second data latch having an input terminal coupled to the output terminal of the first data storage mechanism and an output terminal;

Claims Text - CLTX (26):

a third data latch having an input terminal coupled to the output terminal of the second data latch and an output terminal;

Claims Text - CLTX (27):

an EX-OR logic gate having a first input terminal coupled to the output terminal of the first data storage mechanism, a second input terminal coupled to the output terminal of the third data latch, and an output terminal;

Claims Text - CLTX (30):

a multiplexer having a first input terminal coupled to the output terminal of the high-frequency delay buffer, a second input terminal coupled to the output terminal of the low-frequency delay buffer, an enable coupled to the output terminal of the EX-OR logic gate, and an output terminal; and

Claims Text - CLTX (34):

19. The skew reducer of claim 16, further comprising override circuitry coupled between the output terminal of the EX-OR logic gate and the input terminal of the multiplexer.

Claims Text - CLTX (35):

20. The skew reducer of claim 16, wherein the storage mechanism is selected from the group of storage mechanisms consisting of latches and flip-flops.

	Type	L #	Hits	Search Text	DBs	Time Stamp
21	BRS	L21	3	((signal adj override) near (signal)) and simulation	USPAT	2004/04/15 16:34
22	BRS	L22	47	((signal adj override) and (signal)) and simulation	USPAT	2004/04/15 16:36
23	BRS	L23	0	((signal adj override) and (signal)) near simulation	USPAT	2004/04/15 16:36
24	BRS	L24	47	((signal adj override) and (signal)) and simulation	USPAT	2004/04/15 16:36
25	BRS	L25	0	(signal adj override) and (override near enable) and simulation	USPAT	2004/04/15 16:37
26	BRS	L26	1	(signal adj override) and (enable adj port) and simulation	USPAT	2004/04/15 16:38
27	BRS	L27	0	(signal adj override) and (enable adj port) and simulation and (disable near bit)	USPAT	2004/04/15 16:38
28	BRS	L28	1	(signal adj override) and (enable adj port) and simulation and disable	USPAT	2004/04/15 16:40
29	BRS	L29	72	simulation and (disable adj bit)	USPAT	2004/04/15 16:40
30	BRS	L30	52	simulation and (disable adj bit) and (enable adj bit)	USPAT	2004/04/15 16:41
31	BRS	L31	24	simulation and (disable adj bit) and (enable adj bit) and override	USPAT	2004/04/15 16:41
32	BRS	L32	0	simulation and (disable adj bit) and (enable adj bit) and (override adj signal)	USPAT	2004/04/15 16:41
33	BRS	L33	0	simulation and (disable adj bit) and (enable adj bit) and (override near signal)	USPAT	2004/04/15 16:41
34	BRS	L34	24	simulation and (disable adj bit) and (enable adj bit) and (override and signal)	USPAT	2004/04/15 16:41

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	812	override near circuit	USPAT	2004/04/15 14:53
2	BRS	L2	1148	(override near signal) and circuit	USPAT	2004/04/15 14:53
3	BRS	L3	84	(override near signal) and circuit and simulation	USPAT	2004/04/15 14:54
4	BRS	L4	0	(override near signal) and circuit and simulation and (enable adj bit)	USPAT	2004/04/15 14:54
5	BRS	L5	27	(override near signal) and circuit and simulation and enable and	USPAT	2004/04/15 14:54
6	BRS	L6	27	(override near signal) and circuit and simulation and enable and	USPAT	2004/04/15 14:59
7	BRS	L7	17	(override near signal) and circuit and simulation and enable and disable and latch	USPAT	2004/04/15 15:00
8	BRS	L8	17	(override near signal) and circuit and simulation and enable and disable and latch and override	USPAT	2004/04/15 15:24
9	BRS	L9	901	signal adj override	USPAT	2004/04/15 15:24
10	BRS	L10	47	(signal adj override) and simulation	USPAT	2004/04/15 15:25
11	BRS	L11	20	(signal adj override) and simulation and latch	USPAT	2004/04/15 15:26
12	BRS	L12	0	(signal adj override) and simulation and (disable near bit)	USPAT	2004/04/15 15:26
13	BRS	L13	14	(signal adj override) and simulation and disable and enable and bit	USPAT	2004/04/15 15:27
14	BRS	L14	10	(signal adj override) and simulation and disable and enable and bit and latch	USPAT	2004/04/15 15:27
15	BRS	L15	0	(signal adj override) and simulation and disable and enable and bit and latch and (override near enable)	USPAT	2004/04/15 16:29
16	BRS	L16	150	(override near enable)	USPAT	2004/04/15 15:28
17	BRS	L17	85	(override adj enable)	USPAT	2004/04/15 15:28
18	BRS	L18	5	(override adj enable) and simulation	USPAT	2004/04/15 15:28
19	BRS	L19	0	(override adj enable) and simulation and (override near	USPAT	2004/04/15 15:28
20	BRS	L20	0	(signal adj override) and simulation and "signal versus override"	USPAT	2004/04/15 16:32